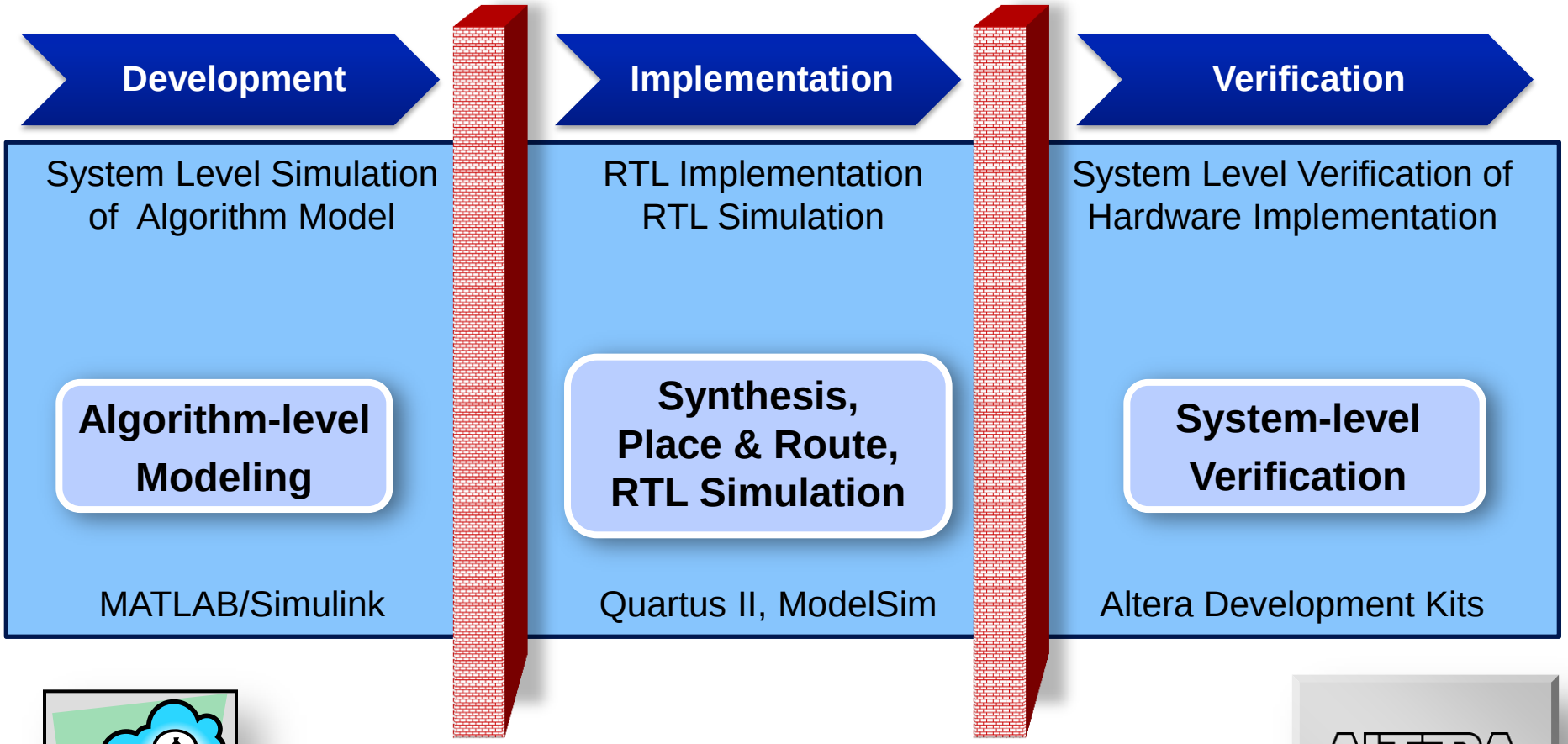
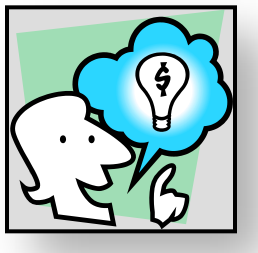
The New Implementation methodology of FPGA

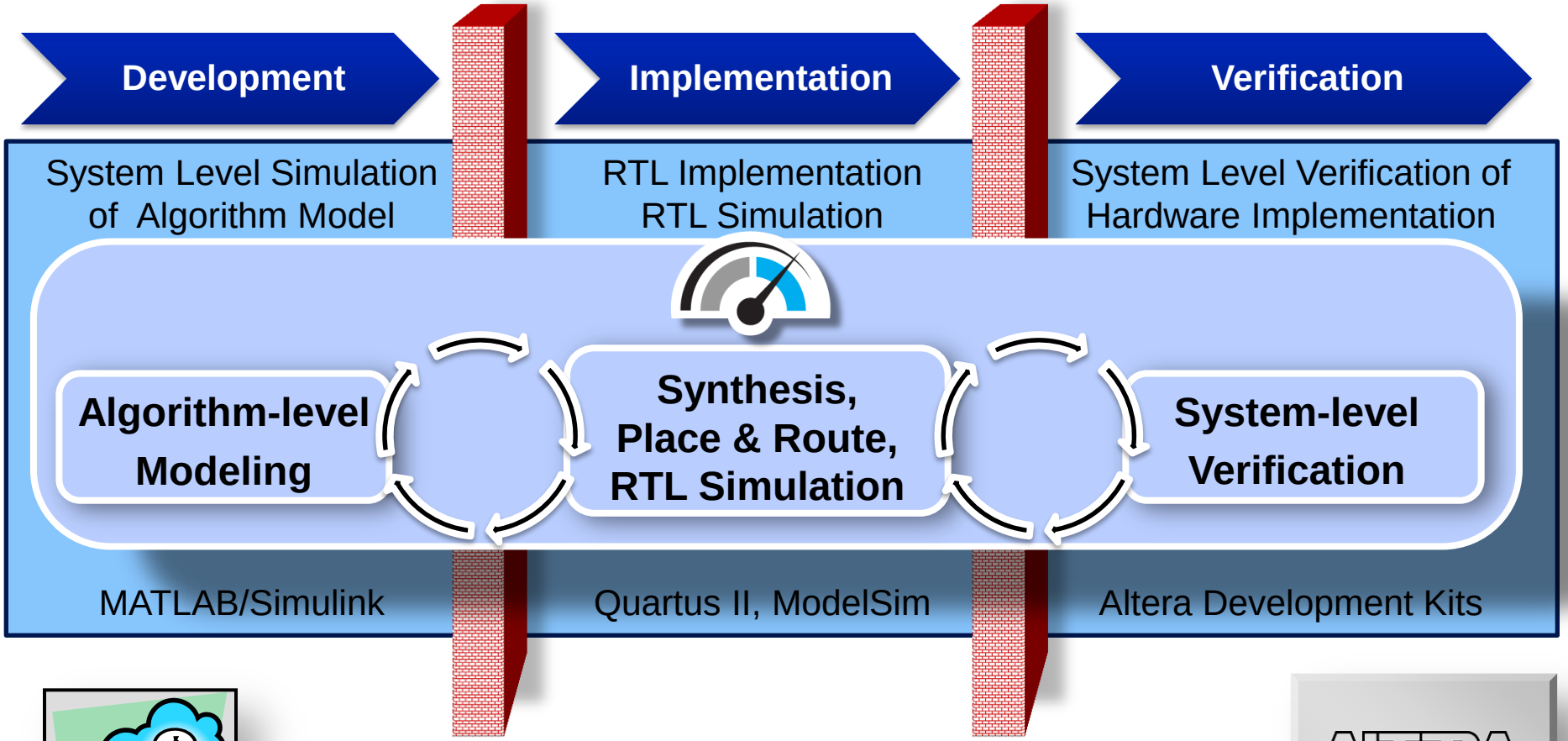
Dylan Wang

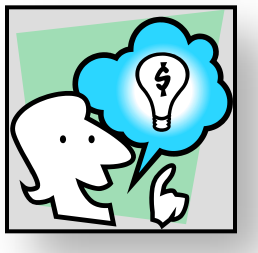
DSP Builder System Level Design Flow





DSP Builder System Level Design Flow





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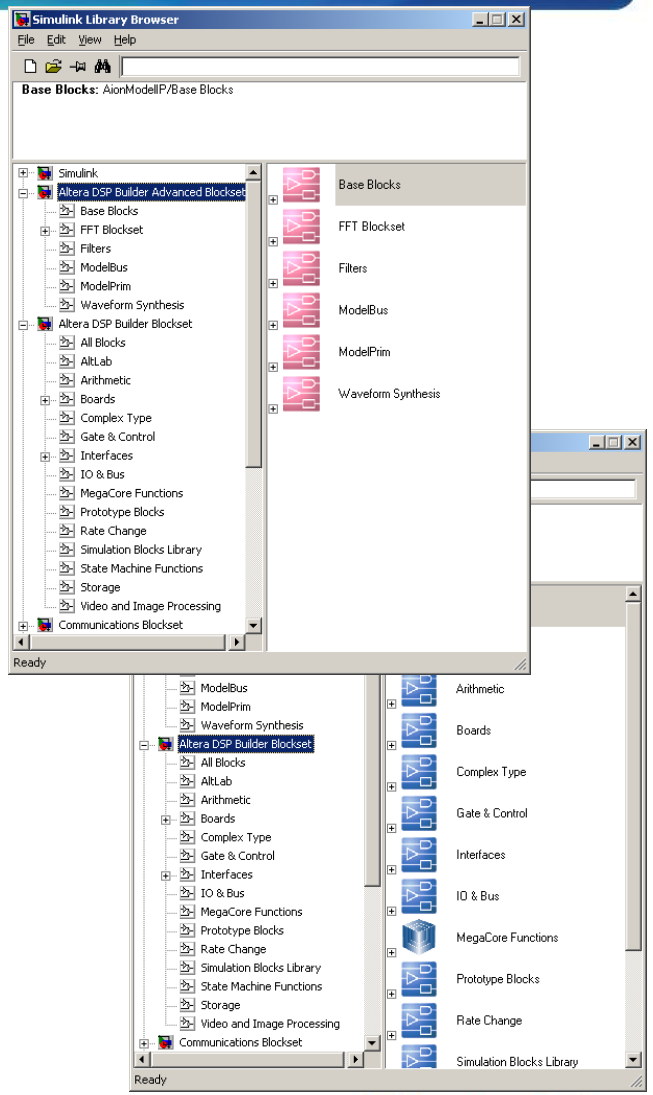
Altera Blockset Libraries

- **DSP Builder Advanced Blockset**
  - **is <u>High Level Synthesis</u> Design**
    - Constraint driven design
    - Abstracted, generic build blocks
    - Single data path logic system clock
    - Automatic pipelining and register balancing
    - High data rate support
    - Floating point support
    - Tool creates the optimized h/w implementation
- **DSP Builder Standard Blockset**
  - **is <u>WYSIWYG</u> design**
    - Structural design
    - Hardware-like building blocks
    - Multiple clock domain design
    - User HDL and DSP IP import
    - Hardware Co-simulation
    - Enables fine-grain control of h/w implementation



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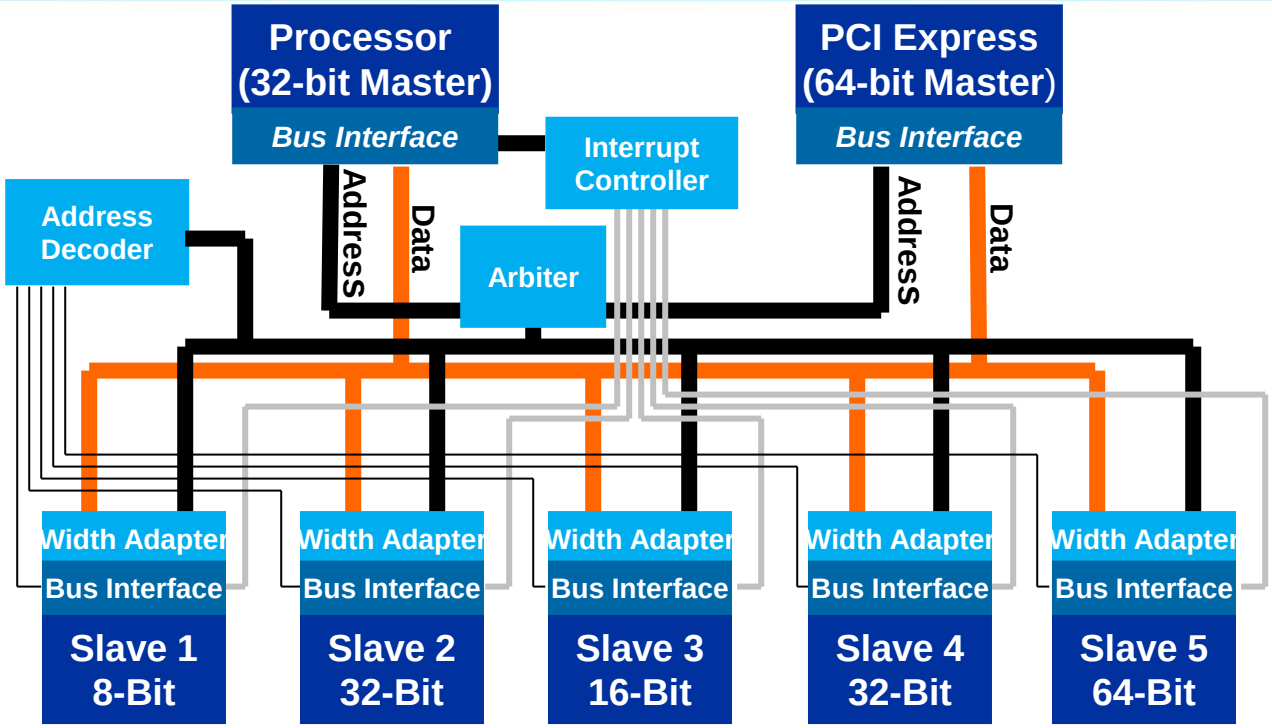
Traditional System Design



- Components in system use different interfaces to communicate (some standard, some non-standard)
- Typical system requires significant engineering work to design custom interface logic
- Integrating design blocks and intellectual property (IP) is tedious and error-prone

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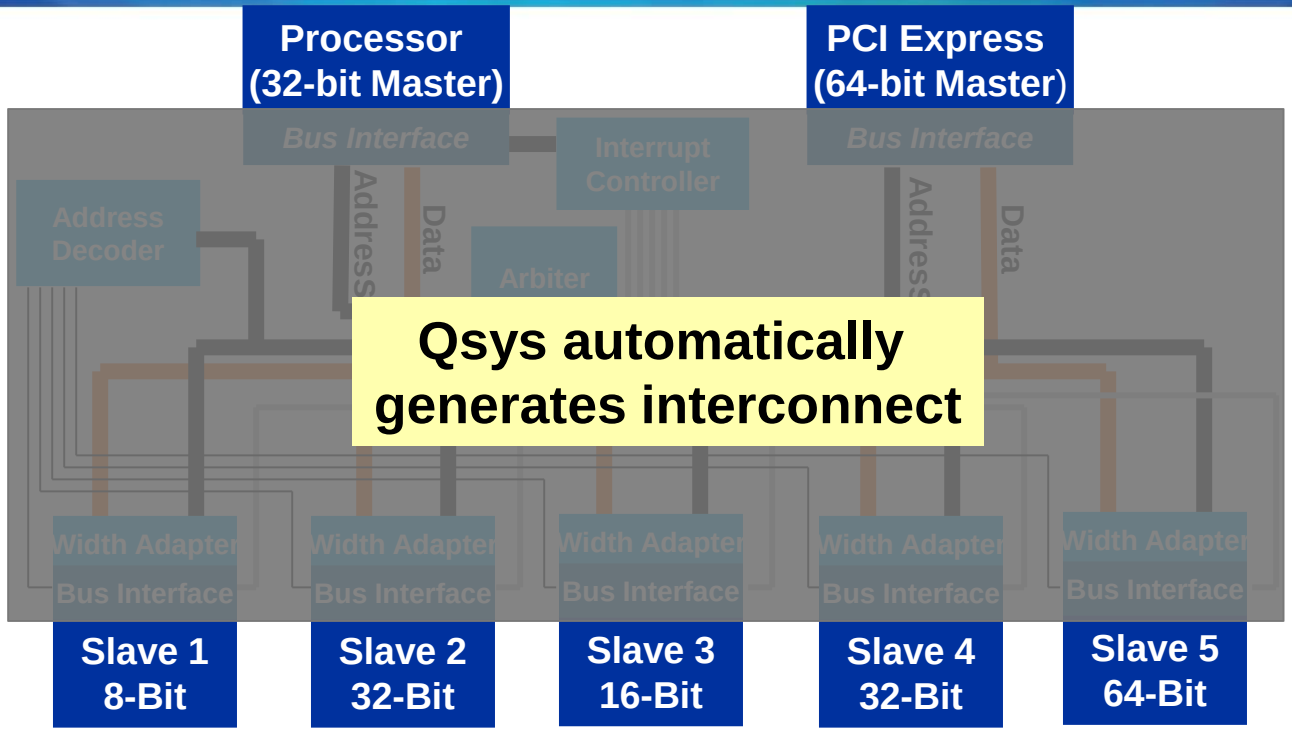
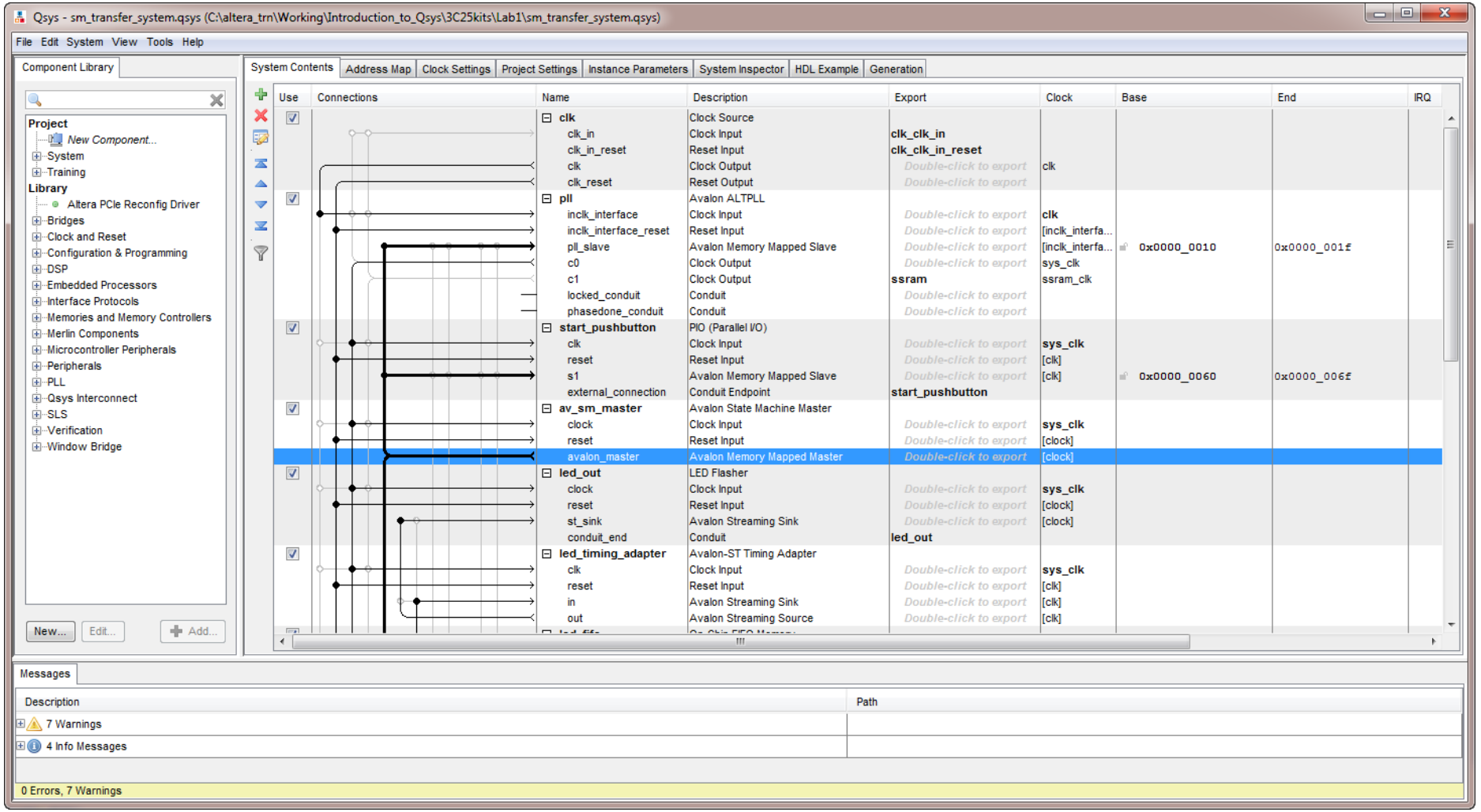
Automatic Interconnect Generation



- Avoids error-prone integration
- Saves development time with automatic logic & HDL generation
- Enables you to focus on value-add blocks

Qsys improves productivity by automatically generating the system interconnect logic

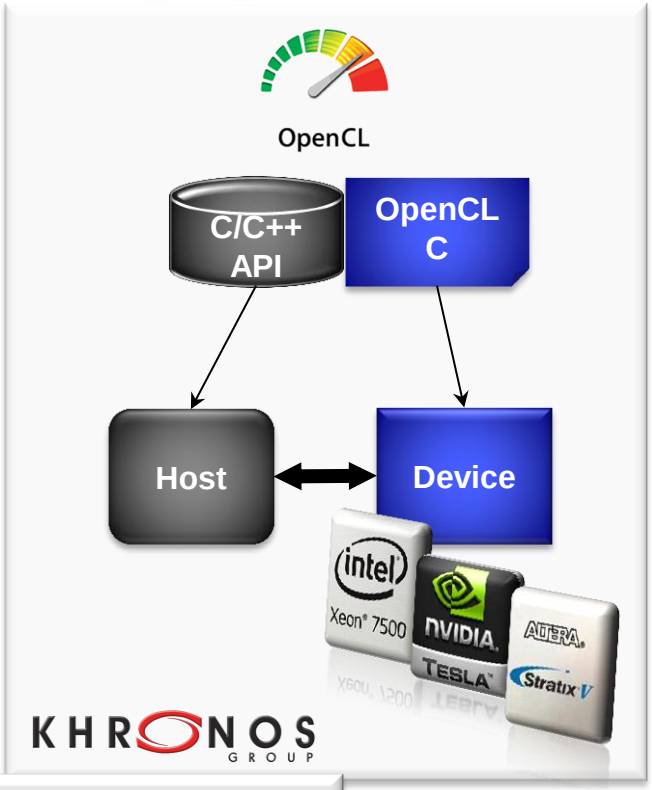
Introducing Qsys



OpenCL (Open Computing Language) Overview

- **Software programming model:**
  - C/C++ API for host program
  - OpenCL C for acceleration device
- **Provides increased performance with hardware acceleration**
  - CPU offload to appropriate accelerator
    - Local Memory
    - Explicit Parallelism
      - Task (SMT)
      - Data (SPMD)

Low Level Programming Language!



- **Open, royalty-free, standard**
  - Managed by Khronos Group
  - Altera active member
  - Conformance requirements
    - V1.0 is current reference
    - V2.0 is current release
  - http://www.khronos.org

KHRONOS GROUP
CONNECTING SOFTWARE TO SILICON
IBM ALTERA intel Google FUJITSU BROADCOM AMD XILINX ARM NVIDIA TEXAS INSTRUMENTS SAMSUNG ELECTRONICS ERICSSON

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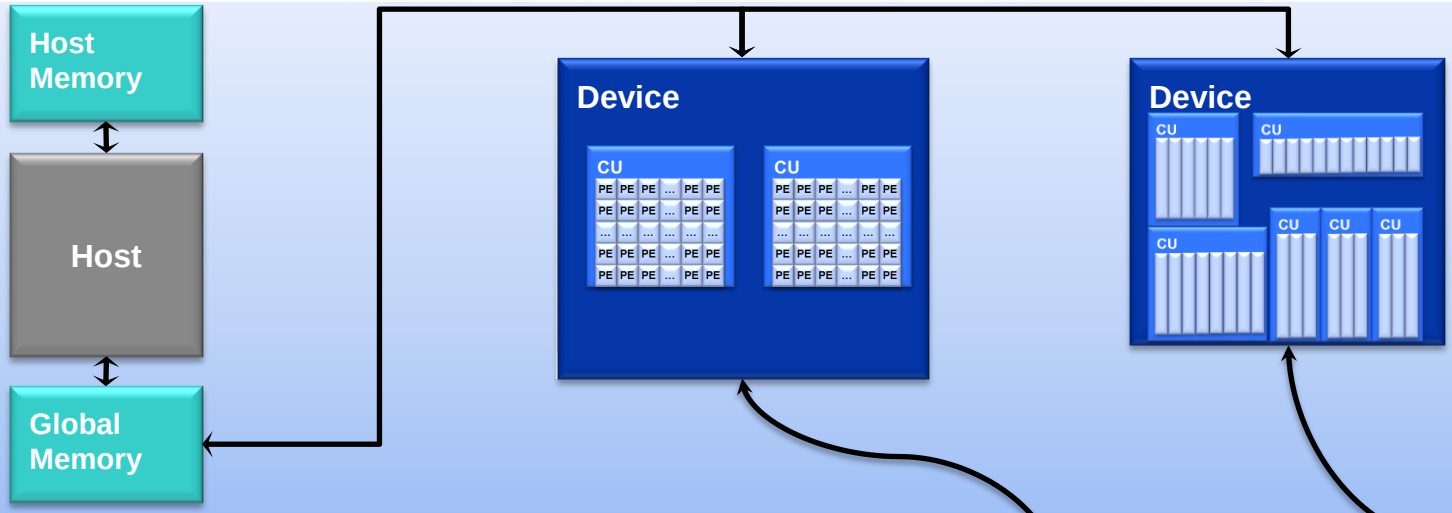
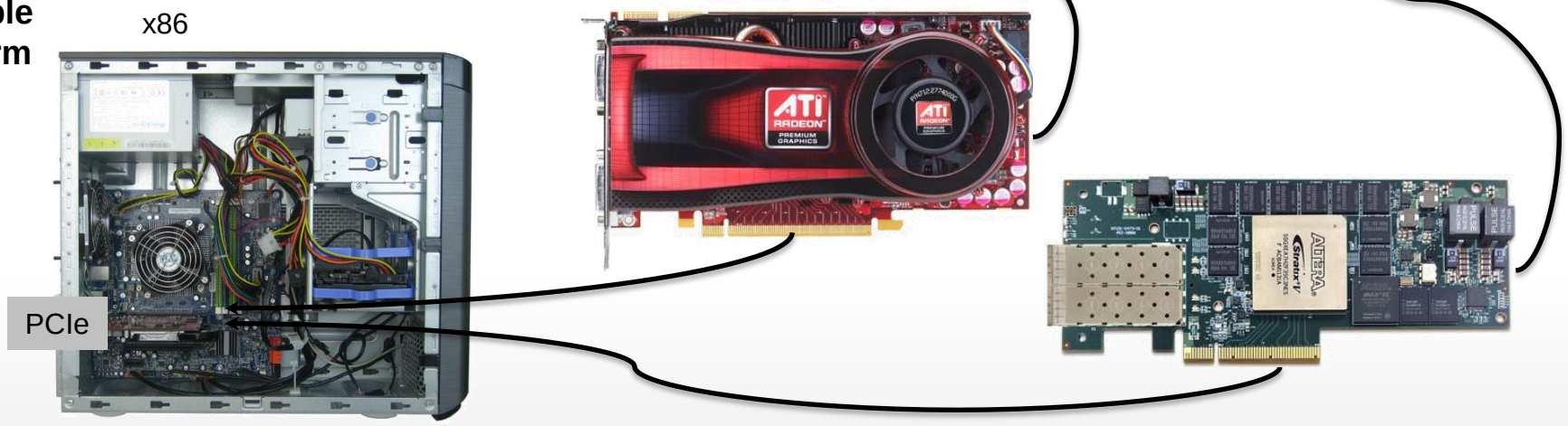
Heterogeneous Platform Model

OpenCL Platform Model



Example Platform



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Use Model: Abstracting the FPGA away

```
main() {
   read_data( … );
   manipulate( … );
   clEnqueueWriteBuffer( … );
   clEnqueueNDRange(…,sum,…);
   clEnqueueReadBuffer( … );
   display_result( … );
}
```

OpenCL
Host Program + Kernels

```
__kernel void sum
   (__global float *a,
    __global float *b,
    __global float *y)
{
  int gid = get_global_id(0);
  y[gid] = a[gid] + b[gid];
}
```

Standard gcc Compiler

Altera Offline Compiler

Verilog

Quartus II

EXE

AOCX

x86

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What happens in future

- Frame work + core processing
- Auto HDL code generating
- Design based on prototype tools and diagram
- Have the chip design without deeply understanding of the device

Thank You

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